## I. AMENDMENT

**In the Claims:**

Please amend the claims as follows:

1. (currently amended) A line selector for a matrix of memory elements, comprising

a plurality of matrix line group selection circuits, each one allowing the selection of a respective group of matrix lines according to a first address, each matrix line group including ~~at least one~~ plurality of matrix lines,

associated with each matrix line group selection circuit, a respective plurality of matrix line selection circuits, each one for allowing the selection of at least one respective matrix line within the respective matrix line group according to a second address, the matrix line selection circuits comprising matrix line driver circuits for driving potentials of the matrix lines,

~~characterized by comprising~~

flag means associated with each matrix line group, that can be set to declare a pending status of a prescribed operation to be conducted globally on the memory elements of the respective matrix line group, the flag means enabling, when set, the execution of the prescribed operation on the respective matrix line group, and

means for entrusting the flag means with the selection of the respective line group during the execution of the prescribed operation, in alternative to the respective line group selection circuit~~, the flag means enabling, when set, the execution of the prescribed operation on the respective line group~~.

2. (original) The line selector according to claim 1, in which the matrix lines are word lines.

3. (original) The line selector according to claim 2, in which the prescribed operation is an erase operation of the memory elements.

4. (original) The line selector according to claim 3, in which the flag means are reset after the respective word line group has been erased.

5. (original) The line selector according to claim 4, in which the flag means are reset after the respective word line group has passed an erase verify operation.

6. (original) The line selector according to claim 5, further comprising setting means and resetting means, associated with each flag means for setting and, respectively, resetting the associated flag means, the setting means and resetting means being enabled by the respective line group selection circuit according to the first address.

7. (original) The word line selector according to claim 2, in which the flag means comprises a set-reset flip-flop.

8. (original) The line selector according to claim 2, in which the means for entrusting the flag means with the selection of the respective line group during the execution of the prescribed operation comprise means for disconnecting the line group selection circuit from a respective line group selection signal line, and means for transferring onto the line group selection signal line a state corresponding to that of the respective flag means.

9. Cancelled.

10. (original) The line selector according to claim 9, in which a word line driver reset circuit is associated with each line group selection circuit, activatable for resetting the word line driver circuits of the associated word line selection circuit.

11. (original) The line selector according to claim 10, in which the word line driver reset circuit, when activated, resets the word line driver circuits of the associated word line selection circuit only if the respective group of word lines is selected.

12. (currently amended) A method of conducting a prescribed operation on a matrix of memory elements, comprising:

providing a matrix line selector having a plurality of matrix line group selection circuits, each matrix line group selection circuit~~one~~ allowing the selection of a respective group of matrix lines according to a~~n~~ first address, each matrix line group including at ~~least one~~ plurality of matrix lines,

providing a plurality of matrix line selection circuits associated with each matrix line group selection circuit, each matrix line selection circuit allowing the selection of at least one respective matrix line within the respective matrix line group according to a second address, the matrix line selection circuits comprising matrix line driver circuits for driving potentials of the matrix lines,

~~characterized by comprising~~

associating with each matrix line group a respective flag,

selectively setting at least one of the flags, to declare a pending status of the prescribed operation to be conducted globally on memory elements of ~~for~~ the respective matrix line group, , the at least one set flag enabling the execution of the prescribed operation globally on memory elements of the respective matrix line group, and

entrusting the flags with the selection of the respective matrix line group, as an alternative to the respective line group selection circuit~~, the at least one set flag enabling the execution of the prescribed operation on the respective matrix line group~~.

13. (original) The method according to claim 12, in which the matrix lines are word lines.

14. (original) The method according to claim 13, in which the prescribed operation is an erase operation.

15. (original) The method according to claim 14, in which the setting of the at least one flag comprises selecting the matrix group via the respective line group selection circuit.

16. (original) The method according to claim 15, further comprising applying at least one erase pulse.

17. (original) The method according to claim 16, further comprising verifying an outcome of the at least one erase pulse by accessing the word lines in the word line group associated with the at least one set flag.

18. (original) The method according to claim 17, in which the verifying further comprises resetting the at least one set flag if the outcome of the at least one erase pulse is positive.

19. (original) The method according to claim 18, in which the resetting the at least one set flag further comprises selecting the associated word line group via the respective line group selection circuit.

20. (original) The method according to claim 19, further comprising applying additional erase pulses and verifying the outcome of each additional erase pulse, until the at least one set flag is reset.

21. (currently amended) A memory comprising a matrix of memory elements and a line selector for selecting lines of the matrix, wherein

~~characterized in that~~

the line selector is realized according to claim 1.

22. (currently amended) A memory~~line selection circuit for selecting a group of lines of an array of memory cells~~, ~~the circuit~~ comprising:

rows of memory cells each coupled to a respective word line, the rows arranged in groups of multiple rows;

status circuits each associated with a respective one of the groups of memory rows and each operable to store a flag that allows a predetermined operation to be performed to the memory cells within the respective group;

a selection circuit coupled to the status circuits and operable to load the flag into selected ones of the status circuits without writing data to the memory cells within the memory-row groups respectively associated with the selected status circuits; ~~select a group of memory cells from the array for an operation~~; and

a control~~status~~ circuit coupled to the groups of memory rows and operable to perform the predetermined operation on only memory cells within the groups of memory rows respectively associated with status circuits that are storing the flag~~selection circuit and operable to enable the selection circuit to perform the operation on a subset of the group of selected memory cells~~.

23. (currently amended) The memory ~~line selector circuit~~ of claim 22 wherein the selection circuit further comprises:

a row address selection circuit operable to select a row of memory cells based upon a first address signal; and

a column address selection circuit operable to select a column of memory cells based upon a second address signal.

24. Cancel

25. (currently amended) The memory~~line selector circuit~~ of claim 22, further comprising a resetting circuit operable to reset the status circuits to a finished state after the operation performed on the memory cells within the associated ~~subset of the~~ groups of ~~selected~~ memory rows~~cells~~ has been verified.

26. – 29. Cancelled

30. (currently amended) An electronic system, comprising:

a memory, including,

rows of memory cells arranged in groups each including multiple rows,

status circuits each associated with a respective one of the groups of rows and each operable to store a flag that allows a predetermined operation to be performed to the memory cells within the respective group,

a selection circuit coupled to the status circuits and operable to load the flag into selected ones of the status circuits without writing data to the memory cells within the groups of memory rows respectively associated with the selected status circuits, and

a control circuit coupled to the groups of memory rows and operable to perform the predetermined operation on only memory cells within the groups of memory rows respectively associated with status circuits that are storing the flag.~~a memory including:~~

~~a line selector circuit having:~~

~~a selection circuit operable to select a group of memory cells from the array for an operation; and~~

~~a status circuit coupled to the selection circuit and operable to enable the selection circuit to perform the operation on a subset of the group of selected memory cells.~~

31. (original) The electronic system of claim 30 wherein the memory comprises an electronic erasable and programmable memory.

32. (currently amended) A method, comprising:

loading a first flag into a storage circuit associated with a group of memory rows without writing data to memory cells within the group; and

performing a first predetermined operation on only memory cells within groups of memory rows associated with respective storage circuits that are storing the flag~~selecting a group of memory elements from an array of memory elements for an operation;~~

~~selecting a subset of the group of memory elements based upon the status of a flag element associated with the memory elements; and~~

~~performing the operation on the subset of the group of memory elements.~~

33. – 35. Cancelled

36. (currently amended) The method of claim ~~35~~32, further comprising:

loading a second flag into the storage circuit after performing the first predetermined operation on the memory cells within the associated group of memory rows; and

performing a second predetermined operation on only the memory cells within the groups of memory rows associated with respective storage circuits that are storing the second flag~~verifying the operation of the operation on each selected memory element;~~

~~setting the status of the flag element to a second status if the operation on the memory element is verified; and~~

~~performing the operation a second time if the operation on the memory element is not verified~~.

37. (currently amended) The method of claim 32 wherein the first predetermined operation comprises an erase operation.

38. (new) The method of claim 32 wherein the second predetermined operation comprises an erase-verify operation.